Nethammer

Inducing Rowhammer Faults through Network Requests

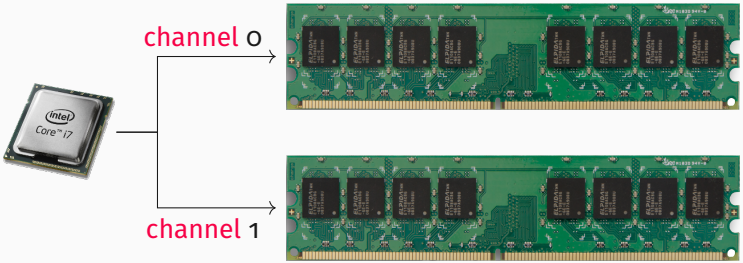
Moritz Lipp[1], Michael Schwarz[1], Lukas Raab[1], Lukas Lamster[1], Misiker Tadesse Aga[2], Clémentine Maurice[3], Daniel Gruss[1]

SILM Workshop 2020

[1]Graz University of Technology, [2] University of Michigan, [3]Univ Rennes, CNRS, IRISA

DRAM organization

DRAM organization



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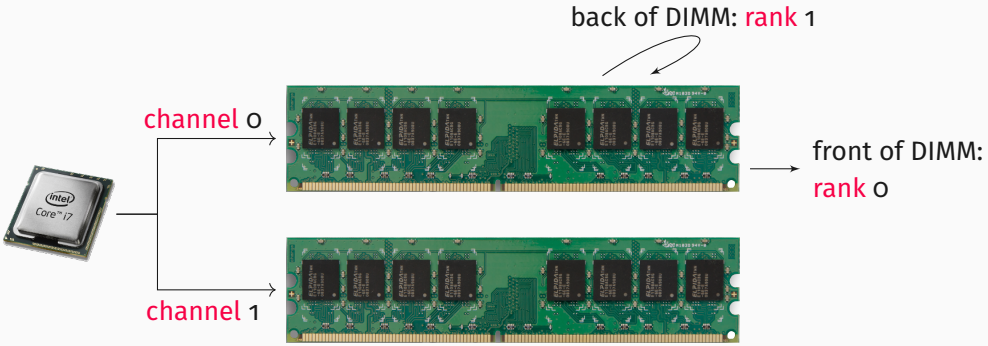

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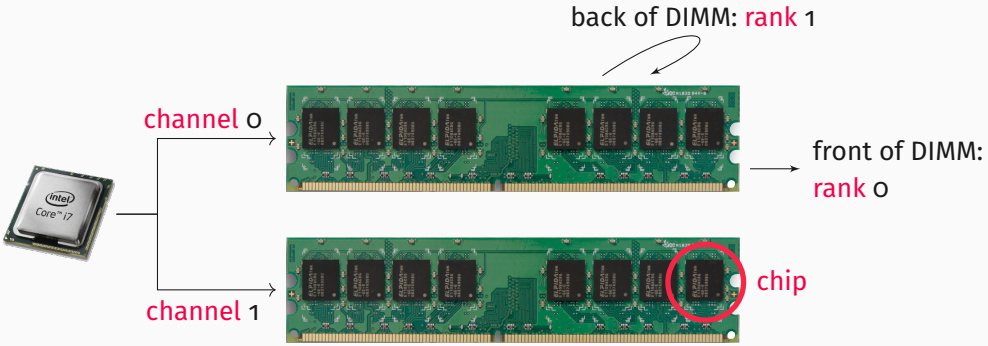
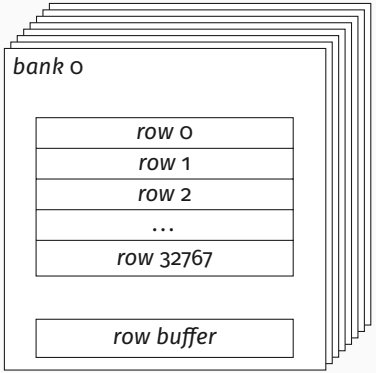


DRAM organization

chip



DRAM organization

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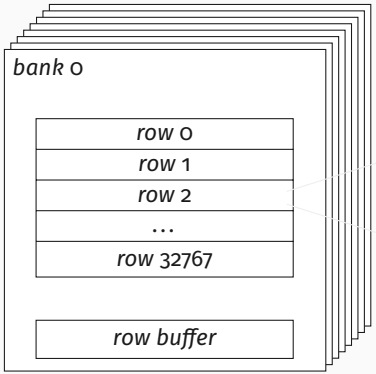
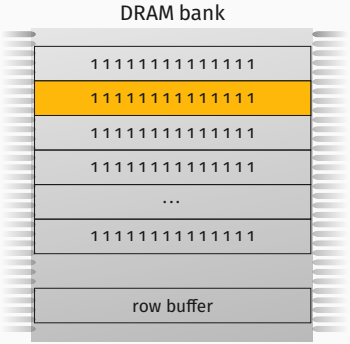


64k cells
1 capacitor,
1 transitor each

How reading from DRAM works



CPU wants to access row 1

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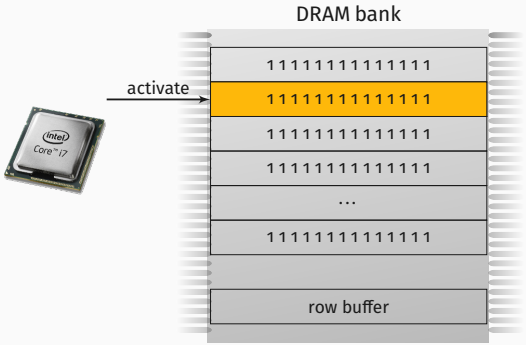

CPU wants to access row 1

$\rightarrow$ row 1 activated

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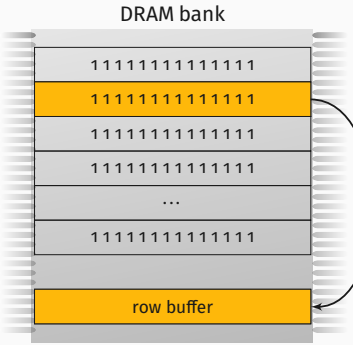

CPU wants to access row 1

$\rightarrow$ row 1 activated

$\rightarrow$ row 1 copied to row buffer

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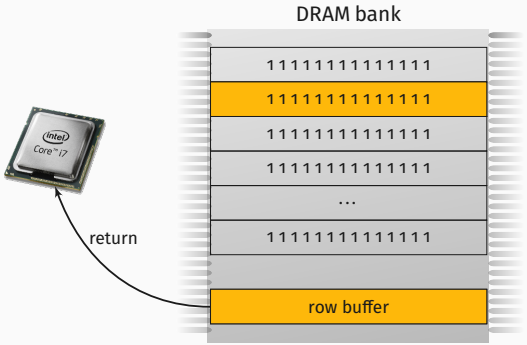

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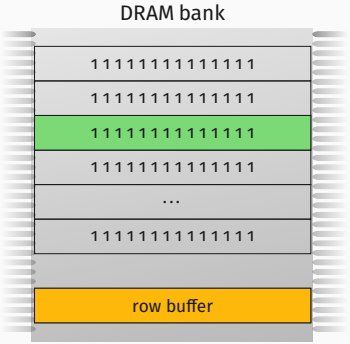
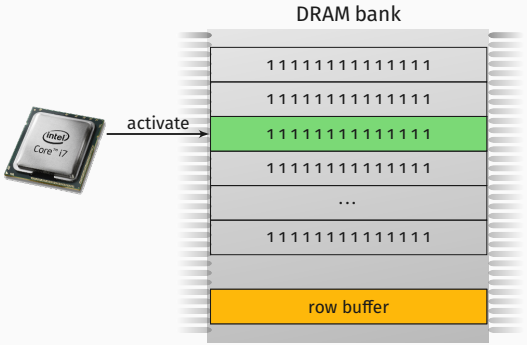


CPU wants to access row 2

How reading from DRAM works



CPU wants to access row 2

$\rightarrow$ row 2 activated

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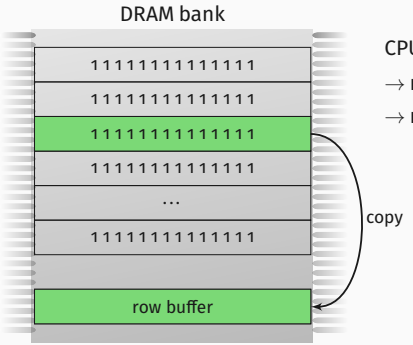

CPU wants to access row 2

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$\rightarrow$ row 2 copied to row buffer

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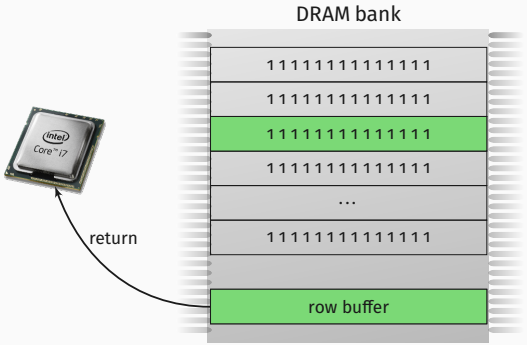

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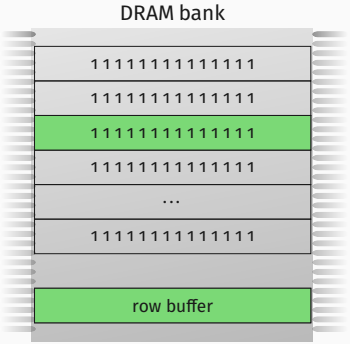


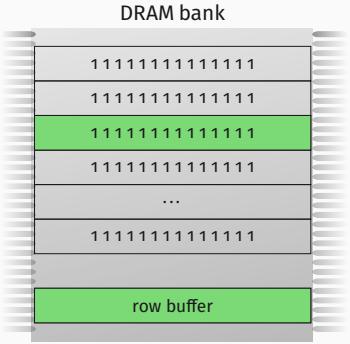
CPU wants to access row 2

→ row 2 activated

→ row 2 copied to row buffer

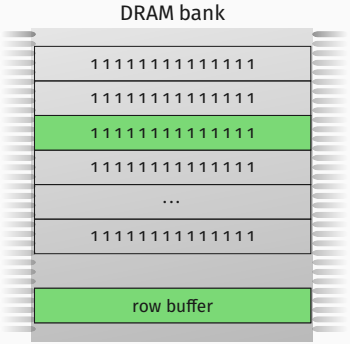
→ slow (row conflict)

How reading from DRAM works



CPU wants to access row 2—again

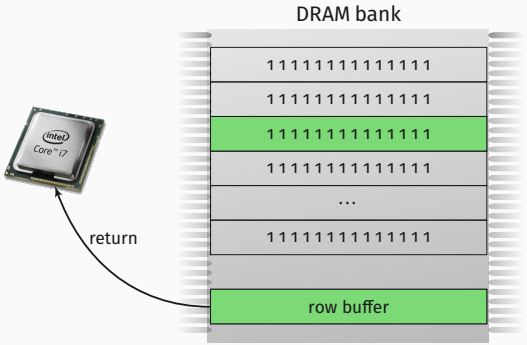
How reading from DRAM works



CPU wants to access row 2—again

$\rightarrow$ row 2 already in row buffer

How reading from DRAM works



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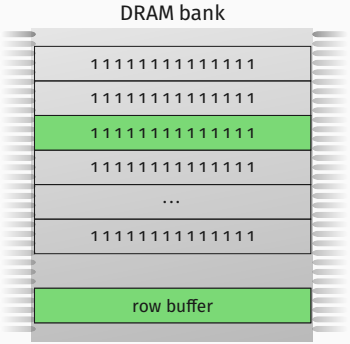
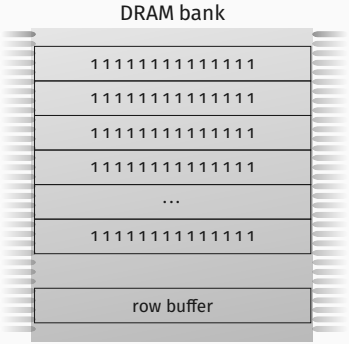


CPU wants to access row 2—again

$\rightarrow$ row 2 already in row buffer

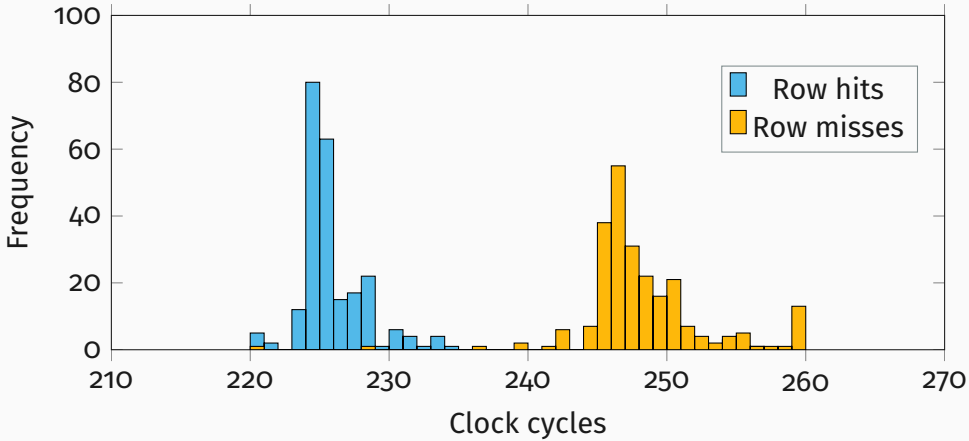
$\rightarrow$ fast (row hit)

How reading from DRAM works

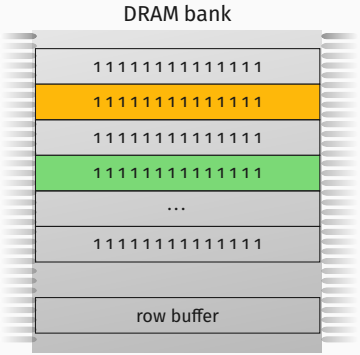


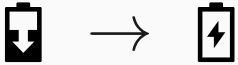
row buffer = cache

Timing difference

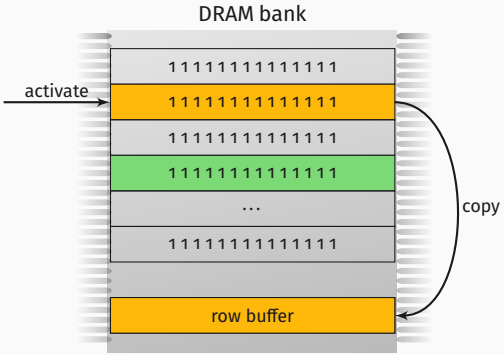


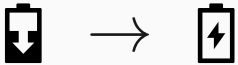
Rowhammer


DRAM bank
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
…
1 1 1 1 1 1 1 1 1 1 1 1 1 1
row buffer



Rowhammer


DRAM bank
activate
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
…
1 1 1 1 1 1 1 1 1 1 1 1 1 1
copy
row buffer



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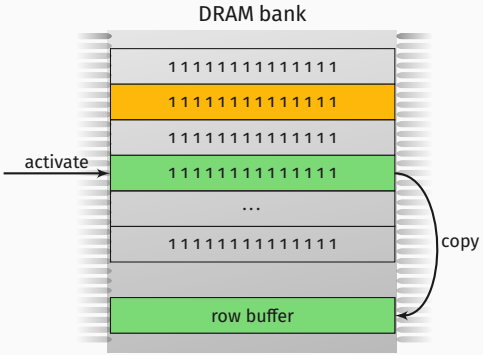
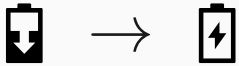
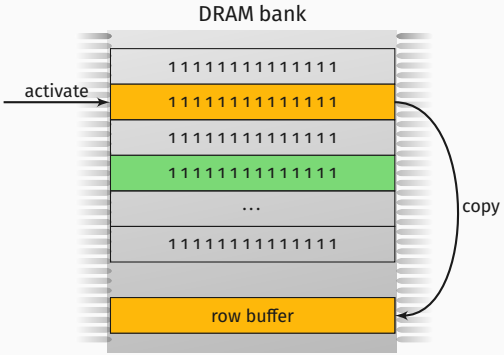
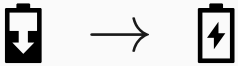




Cells leak faster upon proximate accesses $\rightarrow$ Rowhammer

Rowhammer





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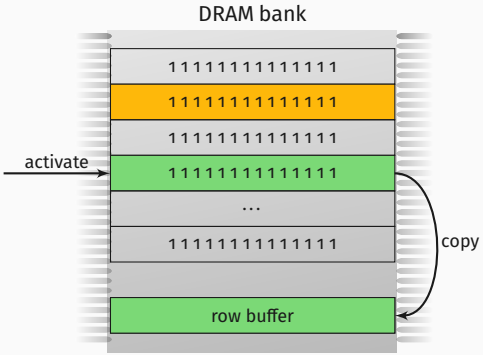

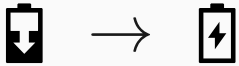

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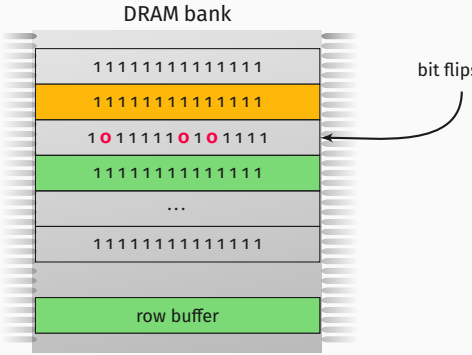
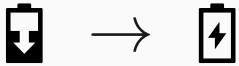


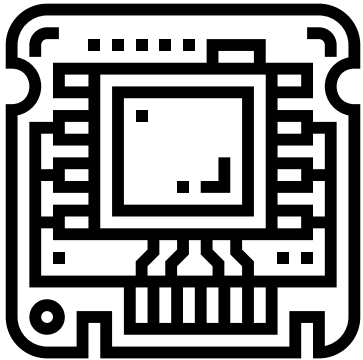


Cells leak faster upon proximate accesses $\rightarrow$ Rowhammer

Requirements

Memory accesses must be

- uncached: reach DRAM
- fast: race against the next row refresh
- targeted: reach specific row



Memory-Controller Policies

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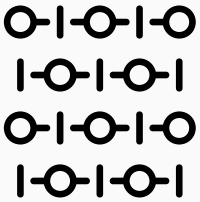
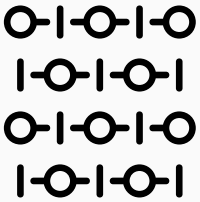


- **Open-page policy**: Keep row opened and buffered

Memory-Controller Policies



- **Open-page policy**: Keep row opened and buffered
  - Low latency for subsequent accesses to same row
  - High latency for accesses to any other row

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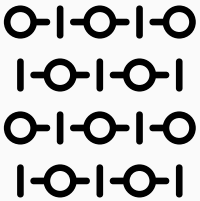

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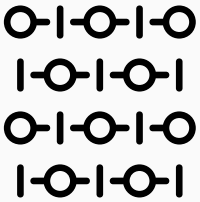

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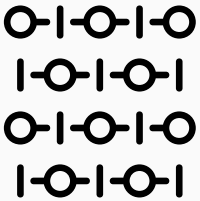

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  - Low latency for subsequent accesses to same row
  - High latency for accesses to any other row
- **Close-page policy**: Immediately close row, ready to open a new row
  - Medium latency for accesses to any row
  - Perform better on multi-core systems [Dav+11]
- **Adaptive-page policy**: Change policy used

Memory-Controller Policies

- Policies that preemptively close rows, would allow one-location hammering

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- We observed close-page policies on desktop computers

Memory-Controller Policies

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- We observed close-page policies on desktop computers
- Mobile devices (e.g., laptops) seem to use mostly open-page policies

Policies

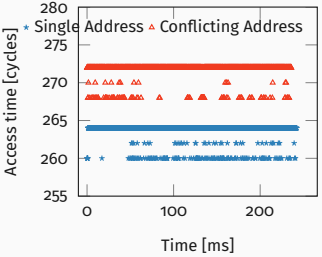


Figure 1: Open

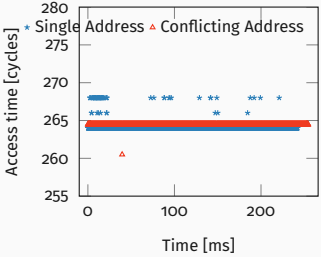


Figure 2: Closed

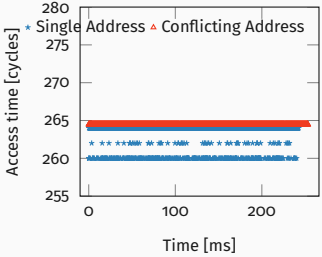
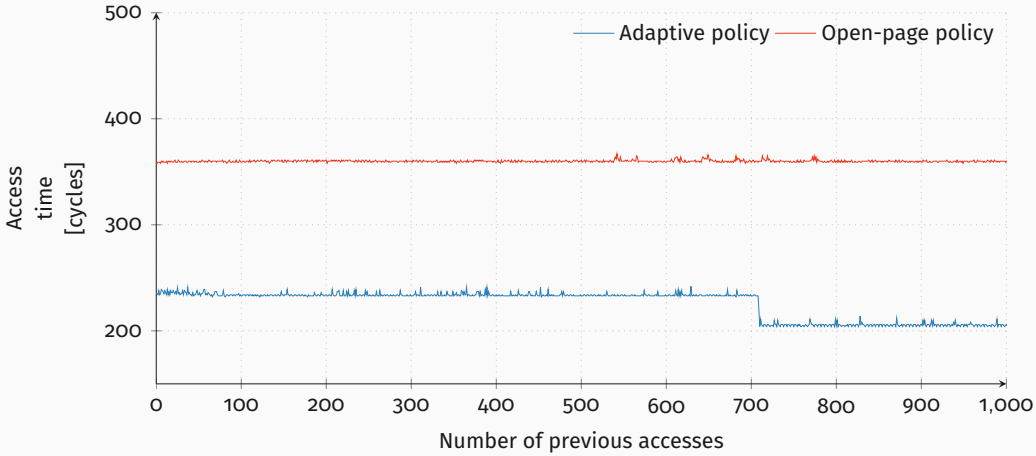
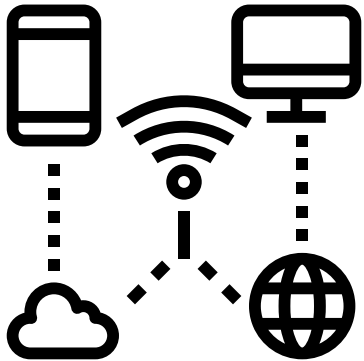


Figure 3: Adaptive

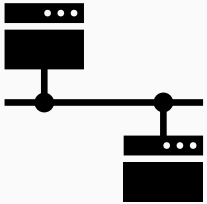
Automated Classification of Memory-Controller Page Policies





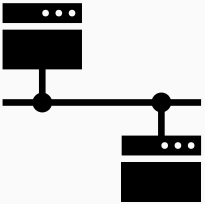
Rowhammer over the Network

Nethammer



- Rowhammer always required local code execution

Nethammer



- Rowhammer always required local code execution
- Rowhammer.js required the victim to visit a website

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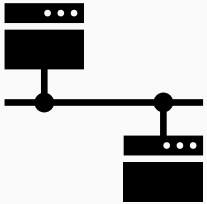
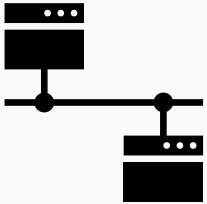


- Rowhammer always required local code execution
- Rowhammer.js required the victim to visit a website
- *Is Rowhammer possible without any attracker-controlled code?*

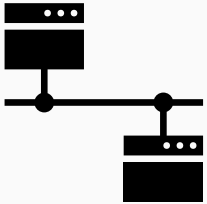
Nethammer



Inducing bit flips:

- Network stacks on ARM often use uncached memory

Nethammer



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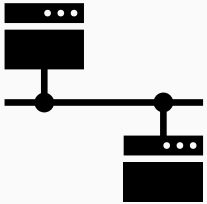

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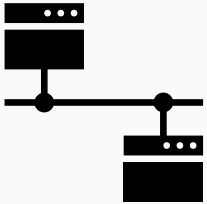

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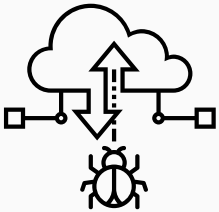
- Network reachable code might use `clflush` or non-temporal stores
- RDMA-enabled Networks (Throwhammer [Tat+18])

Exploiting Nethammer Bit Flips



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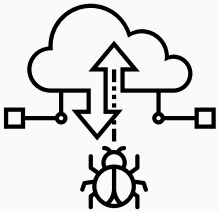

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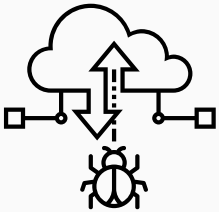

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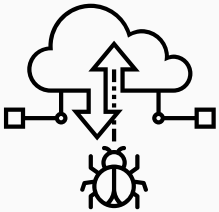

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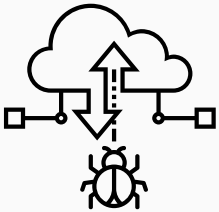

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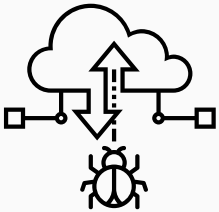

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Setup

- Different CPUs (Desktop, Server, Mobile) with different configurations

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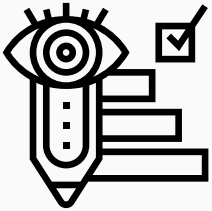
- Monitoring tool that checks for bitflips periodically

Evaluation



- Observed bit flips with different policies used …

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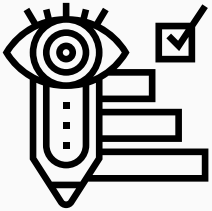

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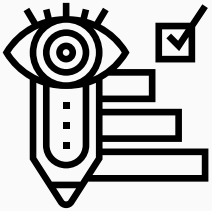

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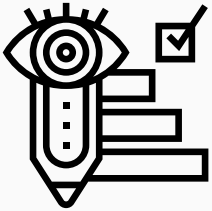

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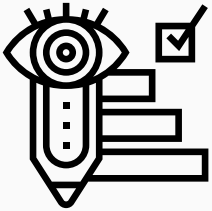

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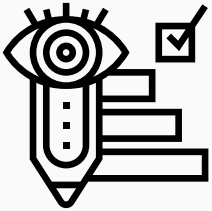

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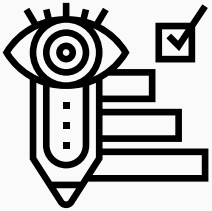

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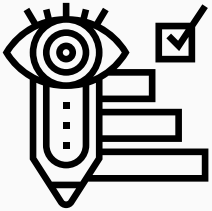

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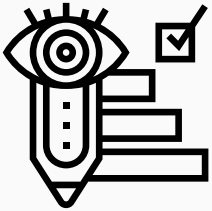

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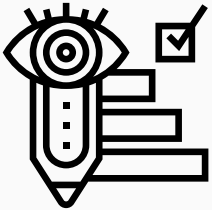

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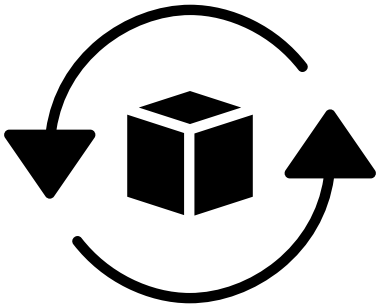
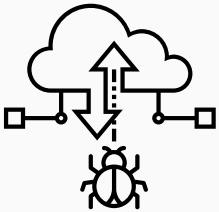


Target Row Refresh (TRR)

TRR



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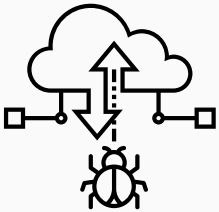

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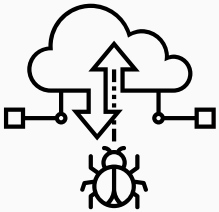

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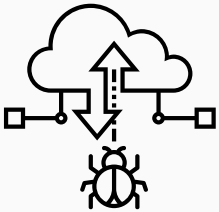

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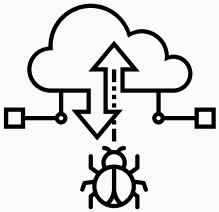

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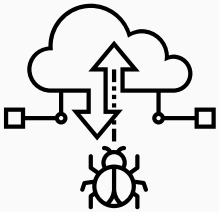

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- Frigo et al. [Fri+20] analyzed TRR in more depth

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Nethammer

Inducing Rowhammer Faults through Network Requests

Moritz Lipp[1], Michael Schwarz[1], Lukas Raab[1], Lukas Lamster[1], Misiker Tadesse Aga[2], Clémentine Maurice[3], Daniel Gruss[1]

SILM Workshop 2020

[1]Graz University of Technology, [2] University of Michigan, [3]Univ Rennes, CNRS, IRISA

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